PATA Disk Module Datasheet

CONTENTS

Revision History

Rev.	Date	History
0.1	2009/4/6	1. 1st draft
0.2	2009/5/13	1. Increase 40 pin PDM SPEC.
0.3	2009/6/4	1. Increase testing data.
0.4	2009/7/29	1. Define form template
0.5	2009/11/11	1. Modify features
0.6	2010/1/7	1. Increase Power Failure Protection description
0.7	2010/4/9	1. Add 1GB solution

1. Overview

Advantech SQFlash PDM (PATA Disk Module) is a non-volatile, solid state data storage disk. Given the advantages of lower power consumption, more rugged, no noise, higher MTBF and other features, PDM is gradually becoming a mainstream to replace conventional Hard Disk Drive. Free of any mechanical components, PDM provides more robust and cost effective storage solution for any embedded application. Offering standard ATA interface, which is fully compatible with traditional HDD, PDM offers designers an easy solution to integrate in PC-based systems.

2. Features

- **Operating Voltage：3.3V、5.0V**
- **Standard ATA/IDE Bus Interface**
  - 512 Bytes/Sector
  - ATA command set compatible
  - Selectable Master/Slave Setting
- **Capacities**
  - SLC type：1GB，2GB，4GB，8GB，16GB
- **Flash type**
  - Only use SLC (single level cell) NAND flash of average 10 times lifecycle and much faster against MLC (multiple level cell)
- **Error Detection / Correction Core (EDC/ECC)**
  - Built-in EDC/ECC up to 12 random bits error per 512 bytes.
- **Wear Leveling**
  - Built-in Static and Dynamic wear leveling function
- **Data Transfer mode**
  - Support Data Transfer up to PIO mode 6
  - Support Data Transfer up to Multiword DMA mode 2
  - Support Data Transfer up to Ultra DMA mode 5
- **Performance**
  - SLC type (Two Chip)
    - Sustain Read Speed up to 40 MB/s
    - Sustain Write Speed up to 29 MB/s
- **Temperature Ranges**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -25℃ to 85℃ for storage
  - Extended Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage
- **Standard Female IDE Connector**
  - 40-pin Vertical
  - 44-pin Horizontal Top
  - 44-pin Horizontal Bottom
  - 44-pin Vertical
  - 44-pin Horizontal
- **Mechanical Specification**
  - Shock：1,500G, Peak / 0.5ms
  - Vibration：20G, Peak / 10~2000Hz

- **Humidty**
  - Operating Humidity：5% ~ 95%
  - Non-Operating Humidity：5% ~ 95%
- **Endurance**
  - SLC type：> 5,000,000 program/erase cycles
- **MTBF**
  - > 6,000,000 hours
- **Data Retention**
  - 10 years
- **Intelligent ATA/IDE Module**
  - Built-in Embedded Flash File System

3. General Description

Advanced NAND Flash Controller

Advantech SQFlash PDM includes Bad Block Management Algorithm, Wear Leveling Algorithm and Error Detection / Correction Code (EDC/ECC) Algorithm.

Bad Block Management

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash PDM implement an efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

Wear Leveling

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash PDM provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

Error Detection / Correction

Advantech SQFlash PDM utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. This algorithm can correct up to 12 random bits per 512 bytes area.

Sophisticate Product Management Systems

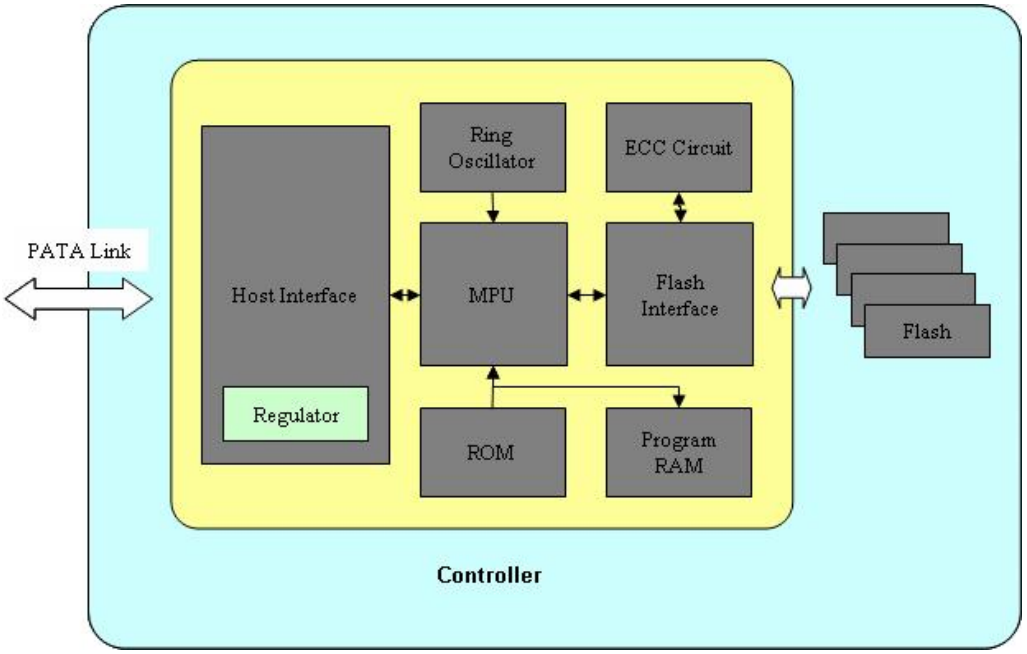
Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

Power Failure Protection

The power detecting level of the controller IC is at 2.9V and that of Flash is at 2.7V. When the power voltage is lower than 2.9V, the controller IC would stop action but Flash still keep running so that can avoid the data written wrong because of the low power voltage.

When the controller IC is writing data and suddenly power failure happens, the controller IC will judge if it completed one page written before power failure; If not, the data of this incomplete page will be written failure.

■ Block Diagram



■ LBA、Cylinders、Heads、Sectors value

Density	LBA (K Bytes)	Cylinders	Heads	Sectors
1 GB	2,006,928	1991	16	63
2 GB	3,940,272	3909	16	63
4 GB	7,880,544	7818	16	63
8 GB	15,761,088	15636	16	63
16 GB	31,522,176	16383	16	63

4. Pin Assignment and Description

4.1 PDM Interface Pin Assignments

Pin #	Signal Name	Pin Type	Pin #	Signal Name	Pin Type
1	-RESET	I	2	GND	-
3	DD7	I/O	4	DD8	I/O
5	DD6	I/O	6	DD9	I/O
7	DD5	I/O	8	DD10	I/O
9	DD4	I/O	10	DD11	I/O
11	DD3	I/O	12	DD12	I/O
13	DD2	I/O	14	DD13	I/O
15	DD1	I/O	16	DD14	I/O
17	DD0	I/O	18	DD15	I/O
19	GND	-	20	KEY_PIN(OPEN)	
21	DMARQ	O	22	GND	-
23	-DIOW:STOP	I	24	GND	-
25	-DIOR:-HDMARDY:HSTOBE	O	26	GND	-
27	IORDY:DDMARDY:DSTROBE		28	CSEL	I
29	-DMACK	I	30	GND	-
31	INTRQ	O	32	IOIS16	O
33	DA1	I	34	-PDIAG:-CBLID	I/O
35	DA0	I	36	DA2	I
37	-CS0	I	38	-CS1	I
39	-DASP	I/O	40	GND	-
41*	VCC	P	42*	VCC	P
43*	GND	-	44*	NC	

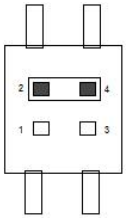
***Note：**

"I"：An input from the host system to the device.
"O"：An output from the device to the host system.
"I/O"：An input/output (bi-direction) common.
"P"：Power supply.
Pin 41~44 only for 44-pin PDM

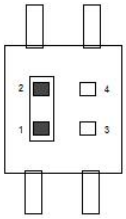
4.2 Jumper Setting

Follow diagram define PDM Master/Slave Jumper (J2) settings

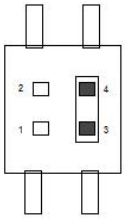
4.2.1 40-pin (H/V) PDM Jumper Settings



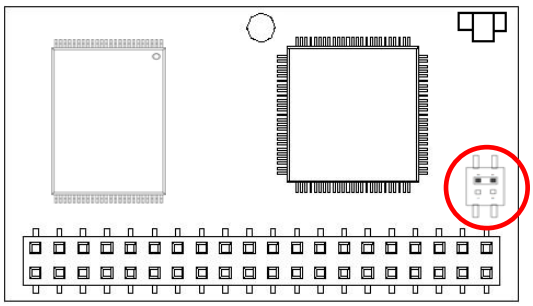
Master



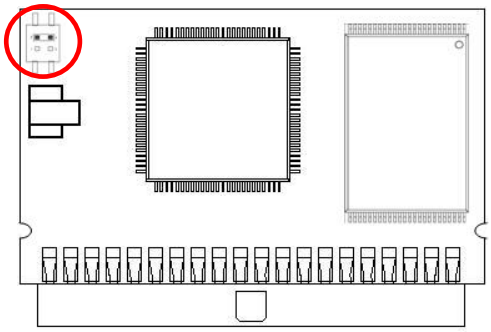
Slave



Cable Select

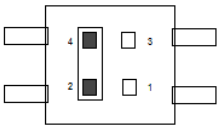


40-pin Horizontal

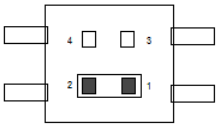


40-pin Vertical

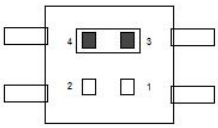
4.2.2 44-pin (H/V) PDM Jumper Settings



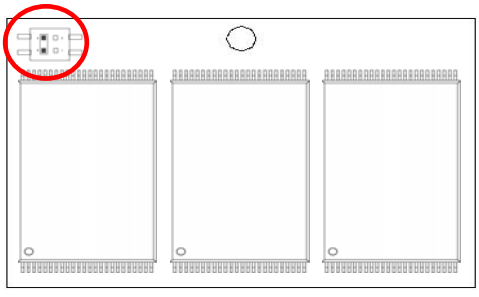
Master



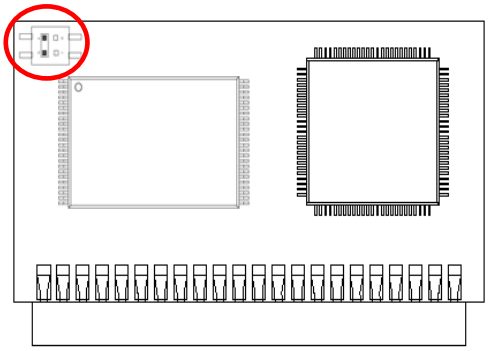
Slave



Cable Select



44-pin Horizontal



44-pin Vertical

4.3 Pin Descriptions

Pin #	Signal Name	Pin Type	Description
1	**-RESET**	I	Hardware reset signal from the host
17, 15, 13, 11, 9, 7, 5, 3, 4, 6, 8, 10, 12, 14, 16, 18	**DD0~DD15** (Device Data)	I/O	16-bit bi-direction Data Bus. DD (7:0) are used for 8-bit register transfers.
21	**DMARQ** (DMA Request)	O	For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.
23	**-DIOW** (I/O Write)	I	This is the strobe signal used by the host to write to the device register or Data port
	STOP (Stop UDMA Burst)		The host assert this signal during an UDMA burst to stop the DMA burst
25	**IORDY** (I/O channel ready)	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
	DDMARDY (UDMA ready)		The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.
	DSTROBE (UDMA data strobe)		When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.
28	**CSEL** (Cable select)	I	This pin is used to configure this device as Device 0 or Device 1.
29	**-DMACK** (DMA acknowledge)	I	This signal is used by the host in respond to DMARQ to initiate DMA transfer.
31	**INTRQ** (Interrupt)	O	When this device is selected, this signal is the active high Interrupt Request to the host
32	**IOIS16**	O	During PIO transfer mode0, 1 or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word. When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted.
35, 33, 36	**DA0~DA2** (Device Address)	I	This is 3-bit binary coded Address Bus.
34	**-PDIAG** (Passed diagnostics)	I/O	This signal will be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics,
	-CBLID (Cable assembly type identify)		
37, 38	**-CS0, -CS1** (Chip select)	I	These signals are used to select the Command Block and Control Block registers. When –DMACK is asserted, -Cs0 and –Cs1 shall be negated and transfers shall be 16-bit wide.
39	**-DASP** (Device active, Device 1 present)	I/O	During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.
41*, 42*	**VCC**	P	Power supply
2, 19, 22, 24, 26, 30, 40, 43*	**GND**	--	Ground.

5. Identify Drive Information

The Identity Drive Command enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration – bit significant for Non-removable device
1	xxxxh	2	Default number of cylinders
2	0000h	2	Reserved
3	xxxxh	2	Default number of heads
4	7E00h	2	Retired
5	0200h	2	Retired
6	xxxxh	2	Default number of sectors per track
7 - 8	xxxxh	4	Number of sectors per device
9	0000h	2	Retired
10 - 19	xxxxh	20	Serial Number in ASCII
20	0002h	2	Retired
21	0002h	2	Retired
22	0004h	2	Number of ECC Bytes passed on Read/Write Long Commands
23 - 26	aaaah	8	Firmware revision in ASCII
27 - 46	xxxxh	40	Model number in ASCII
47	8001h	2	Maximum number of sector that shall be transferred on Read/Write Multiple commands
48	0000h	2	Reserved
49	2B00h	2	Capabilities-LBA/DMA Supported
50	4000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Retired
53	0007h	2	Word 54 - 58, 64 - 70 and 88 are valid
54	xxxxh	2	Current numbers of cylinders
55	xxxxh	2	Current numbers of heads
56	xxxxh	2	Current sectors per track
57 - 58	xxxxh	4	Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)
59	0101h	2	Multiple sector setting is valid
60 - 61	xxxxh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Retired
63	0007h	2	Multiword DMA mode 2 and below are supported
64	0003h	2	Advance PIO transfer modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time 120nsec
66	0078h	2	Manufacturer's recommended Multiword DMA transfer cycle time 120nsec
67	0078h	2	Minimum PIO transfer cycle time without flow control 120nsec
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control 120 nsec
69 - 79	0000h	26	Reserved
80	0030h		Major version number
81	0000h		Reserved
82	7009h	2	Supports Security Mode feature set
83	5004h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
84	4000h		
85	7009h		Feature Setting
86	1004h		Feature Setting
87	4000h		Feature Setting
88	203Fh	2	Ultra DMA mode 5 and below are supported, UDMA mode5 select
89 - 92	0000h	8	Reserved
93	xxxxh		
94 - 128	0000h	2	Enhanced security erase supported
129 - 159	0000h	62	Reserved vendor unique bytes
160 - 255	0000h	192	Reserved

***Note：**

“a”： Vender Specific Configuration

“n”： Host Selectable Configuration

6. Power Management

PDM provides automatic power saving mode. There are four modes on this system.

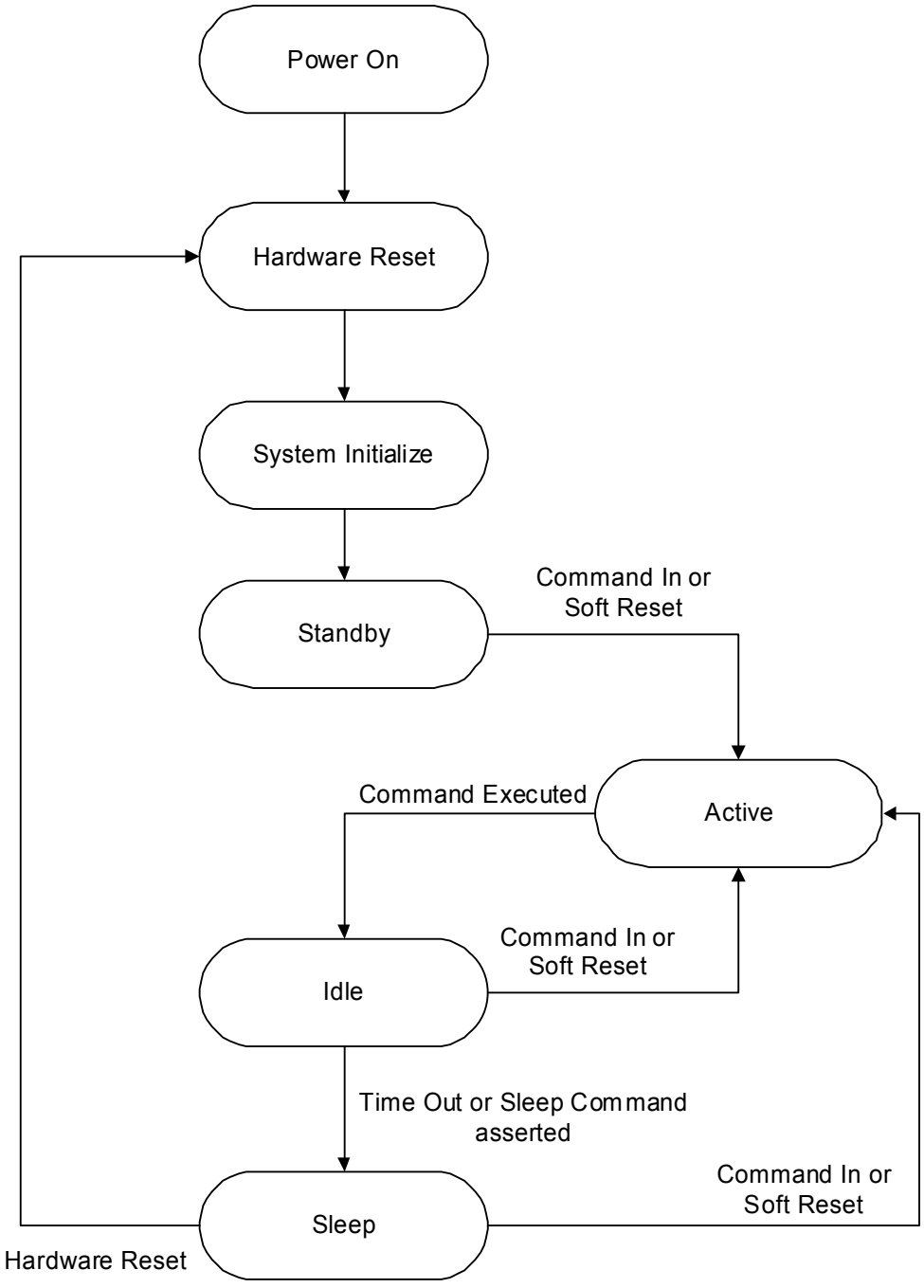
Standby Mode: When PDM finishes the initialization routine after power reset, it goes into Standby Mode and wait for Command In or Soft Reset.

Active Mode: If PDM received any Command In or Soft Reset, it goes into Active Mode. In Active Mode, it is capable to execute any ATA commands. The power consumption is the greatest in this mode.

Idle Mode: After PDM executed any ATA Commands or Soft Reset, it goes into Idle Mode. Power consumption is reduced from Active Mode.

Sleep Mode: The PDM will enter Sleep Mode if there is no Command In or Soft Reset from the host. Sleep Mode provides the lowest power consumption. During Sleep Mode, the system main clock is stopped. This mode can be waked up from hardware reset, software reset or any ATA command asserted.

6.1 Power Saving Flow



7. ATA Command Set

[Command Set List]

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	CHECK POWER MODE	98h,E5h	N	N	N	N	Y	N	N
2	EXECUTE DEVICE DIAGNOSTIC	90h	N	N	N	N	N	N	N
3	IDENTIFY DEVICE	Ech	N	N	N	N	Y	N	N
4	IDLE	97h,E3h	N	Y	N	N	Y	N	N
5	IDLE IMMEDIATE	95h,E1h	N	N	N	N	Y	N	N
6	INITIALIZE DEVICE PARAMETERS	91h	N	Y	N	N	Y	Y	N
7	NOP	00h	N	N	N	N	Y	N	N
8	READ BUFFER	E4h	N	N	N	N	Y	N	N
9	READ DMA	C8h,C9h	N	Y	Y	Y	Y	Y	Y
10	READ MULTIPLE	C4h	N	Y	Y	Y	Y	Y	Y
11	READ NATIVE MAX ADDRESS	F8h	N	N	N	N	Y	N	Y
12	READ LONG SECTOR	22h,23h	N	N	Y	Y	Y	Y	Y
13	READ SECTOR(S)	20h,21h	N	Y	Y	Y	Y	Y	Y
14	READ VERIFY SECTOR(S)	40h,41h	N	Y	Y	Y	Y	Y	Y
15	RECALIBRATE	1Xh	N	N	N	N	Y	N	N
16	SECURITY DISABLE PASSWORD	F6h	N	N	N	N	Y	N	N
17	SECURITY ERASE PREPARE	F3h	N	N	N	N	Y	N	N
18	SECURITY ERASE UNIT	F4h	N	N	N	N	Y	N	N
19	SECURITY FREEZE LOCK	F5h	N	N	N	N	Y	N	N
20	SECURITY SET PASSWORD	F1h	N	N	N	N	Y	N	N
21	SECURITY UNLOCK	F2h	N	N	N	N	Y	N	N
22	SEEK	7Xh	N	N	Y	Y	Y	Y	Y
23	SET FEATURE	EFh	Y	Y	Y	Y	Y	Y	N
24	SET MULTIPLE	C6h	N	Y	N	N	Y	N	N
25	SLEEP	99h,E6h	N	N	N	N	Y	N	N
26	SMART ENABLE/DISABLE AUTO SAVE	B0h	D2h	Y	N	Y	Y	N	N
27	SMART ENABLE OPERATION	B0h	D8h	N	N	Y	Y	N	N
28	SMART DISABLE OPERATION	B0h	D9h	N	N	Y	Y	N	N
29	SMART RETURN STATUS	B0h	DAh	N	N	Y	Y	N	N
30	STANDBY	96h,E2h	N	N	N	N	Y	N	N
31	STANDBY IMMEDIATE	94h,E0h	N	N	N	N	Y	N	N
32	WRITE BUFFER	E8h	N	N	N	N	Y	N	N
33	Write DMA	CAh,CBh	N	Y	Y	Y	Y	Y	Y
34	Write Multiple	C5h	N	Y	Y	Y	Y	Y	Y
35	Write Long Sector	32h,33h	N	N	Y	Y	Y	Y	Y
36	Write Sector(s)	30h,31h	N	Y	Y	Y	Y	Y	Y
37	Write Verify	3Ch	N	Y	Y	Y	Y	Y	Y

Note : FR: Feature Register
SC: Sector Count registers
SN: Sector Number register
CY: Cylinder Low/High register
DR: Device bit of Device/Head register
HD: Head No. (3 to 0) of Device/Head register
NH: No. of Heads
LBA: Logical Block Address
Y: Setup
N: Not setup

[Command Set Descriptions]

1. CHECK POWER MODE (code: E5h);
This command checks the power mode.

2. EXECUTE DEVICE DIAGNOSTIC (code: 90h);
This command performs the internal diagnostic tests implemented by the module.

3. IDENTIFY DEVICE (code: ECh);
The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

4. IDLE (code: 97h or E3h);
This command allows the host to place the module in the Idle mode and also set the Standby timer. H_INTRQ_P may be asserted even through the module may not have fully transitioned to Idle mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

5. IDLE IMMEDIATE (code: 95h or E1h);
This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

6. INITIALIZE DEVICE PARAMETERS (code: 91h);
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

7. NOP (code: 00h);
If this command is issued, the module respond with command aborted.

8. READ BUFFER (code: E4h);
This command enables the host to read the current contents of the module's sector buffer.

9. READ DMA (code: C8h,C9h);
This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

10. READ MULTIPLE (code: C4h);
This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple commands.

11. READ NATIVE MAX ADDRESS (code: F8h);
This command returns the native maximum address.

12. READ LONG SECTOR (code: 22h, 23h);
This command is provided for compatibility purposes and nearly performs "1" sector READ SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are all 0 data.

13. READ SECTOR(S) (code: 20h or 21h);
This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

14. READ VERIFY SECTOR(S) (code: 40h or 41h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

15. RECALIBRATE (code: 1Xh);

This command return value is select address mode by the host request.

16. SECURITY DISABLE PASSWORD (code: F6h);

This command transfers 512Bytes of data from the host. Table Security Password defines the content of this information.

17. SECURITY ERASE PREPARE (code: F3h);

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlock. This command prevents accidental erase of the device.

18. SECURITY ERASE UNIT (code: F4h);

This command requests transfer of a single sector of data as form of table SECURITY ERASE UNIT password from the host.

If the password is not match, this command will be reject, the Security Erase Prepare command should be completed immediately prior the Security Erase Unit command.

If Normal Erase mode, the all user data area will be written binary 0, if Enhanced Erase mode, the predetermined data pattern will written to the user data area.

19. SECURITY FREEZE LOCK (code: F5h);

This command sets the device to Frozen mode. After command completion, all other commands that update device lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset.

20. SECURITY SET PASSWORD (code: F1h);

This command requests a transfer of a single sector of data from the host.

21. SECURITY UNLOCK (code: F2h);

This command requests transfer of a single sector of data from the host.

22. SEEK (code: 7Xh);

This command performs a range check.

23. SET FEATURE (code: EFh);

This command is used by the host to establish parameters that affect the execution of certain device features.

24. SET MULTIPLE MODE (code: C6h);

This command enables the module to perform READ and Write Multiple operations and establishes the block count for these commands.

25. SLEEP (code: 99h or E6h);

This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

26. SMART ENABLE/DISABLE AUTO SAVE (code: B0h);

This command enables and disables the optional attribute auto save feature of the module.

27. SMART ENABLE OPEARIONS (code: B0h);
This command enables access to all SMART capabilities within the module.

28. SMART DISABLE OPEMTIONS (code: B0h);
This command disables all SMART capabilities within the module.

29. SMART RETURN STATUS (code: B0h);
This command causes the module return the reliability status of the module to the host.

30. STANDBY (code: 96h or E2h);
This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

31. STANDBY IMMEDIATE (code: 94h or E0h);
This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.

32. WRITE BUFFER (code: E8h);
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

33. WRITR DMA (code: CAh or CBh);
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

34. WRITE MULTIPLE (code: C5h);
This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

35. WRITE LONG SECTOR (code: 32h or 33h);
This command is provided for compatibility purposes and nearly performs "1" sector WRITE SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are not written on the flash memories.

36. WRITE SECTOR(S) (code: 30h or 31h);
This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

37. WRITE VERIFY (code: 3Ch);
This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

8. System Power Consumption

(Ta = 0 to 70℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Iccr	Read current	5V	-	100	-	mA
Iccw	Write current	5V	-	105	-	mA
Ipd	Power down current	5V	-	0.2	0.4	mA
Iccr	Read current	3.3V	-	150	-	mA
Iccw	Write current	3.3V	-	160	-	mA
Ipd	Power down current	3.3V	-	0.3	-	mA

9. Electrical Specifications

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Remark
V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V	
V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V	
Ta	Operating Temperature	0	+70	℃	Commercial version
Tst	Storage Temperature	-25	+85	℃	Commercial version
Ta	Operating Temperature	-40	+85	℃	Extended version
Tst	Storage Temperature	-40	+85	℃	Extended version

Symbol	Parameter	Min	Typ	Max	Unit	Remark
V_{DD}	V_{DD} Voltage	3.0	3.3	3.6	V	
		4.5	5.0	5.5	V	

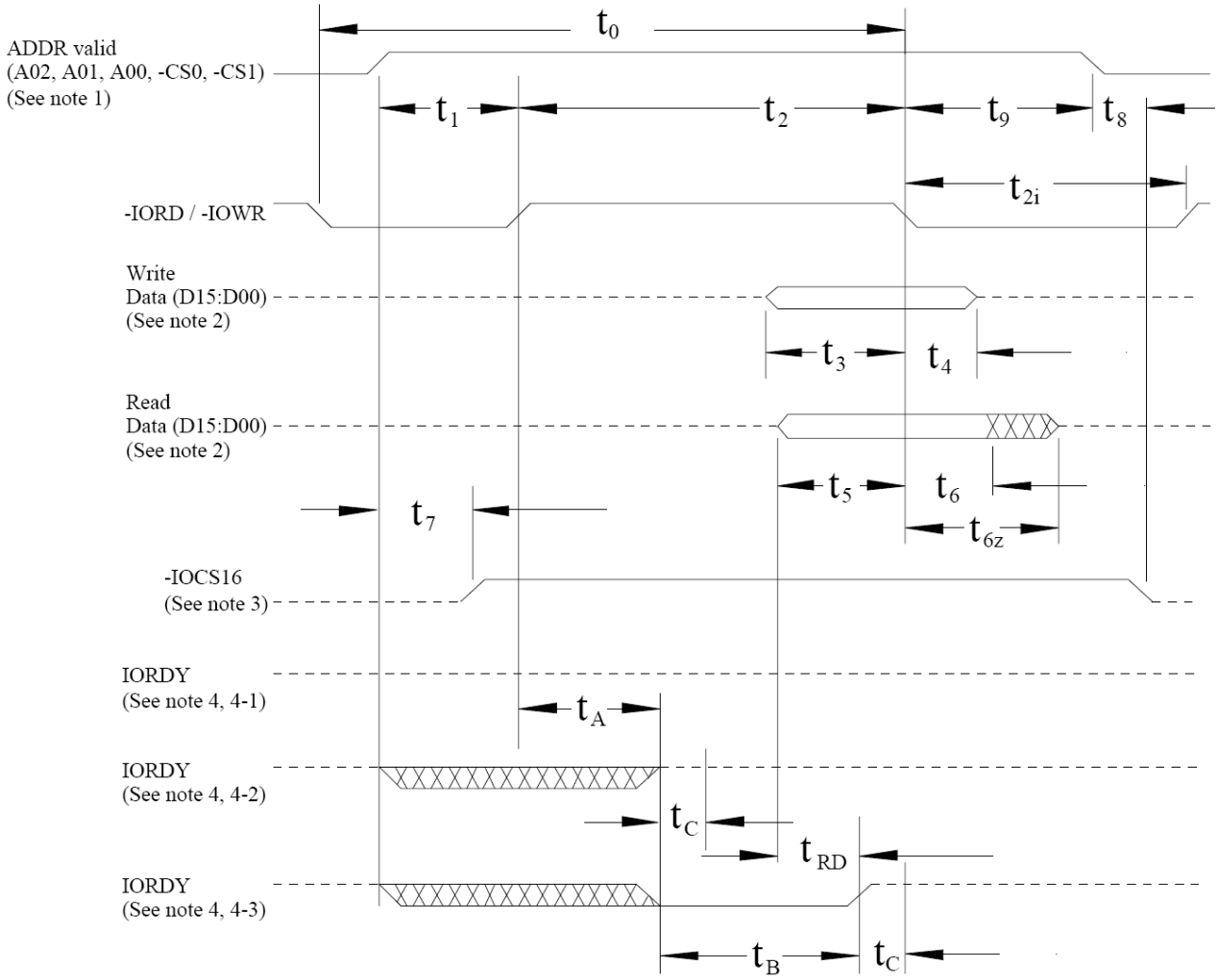
10. DC Characters

DC characteristics of 5.0V I/O Cells (Host Interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vol	Output Low Voltage	|Iol| = 4 ~ 32 mA	-	-	0.4	V
Voh	Output High Voltage	|Ioh| =4 ~ 32 mA	2.4	-	-	V
Vil	Input Low Voltage	TTL (5V)	-	-	0.85	V
Vih	Input High Voltage		1.25	-	-	V
Vil	Input Low Voltage	TTL (3.3V)	-	-	1.05	V
Vih	Input High Voltage		1.75	-	-	V
Iin	Input Leakage Current	No pull-up or pull-down	-10	±1	10	µA
Ioz	Tri-state Output Leakage Current		-10	±1	10	µA

11. AC Characters

11.1 PIO Data Transfer



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	

tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

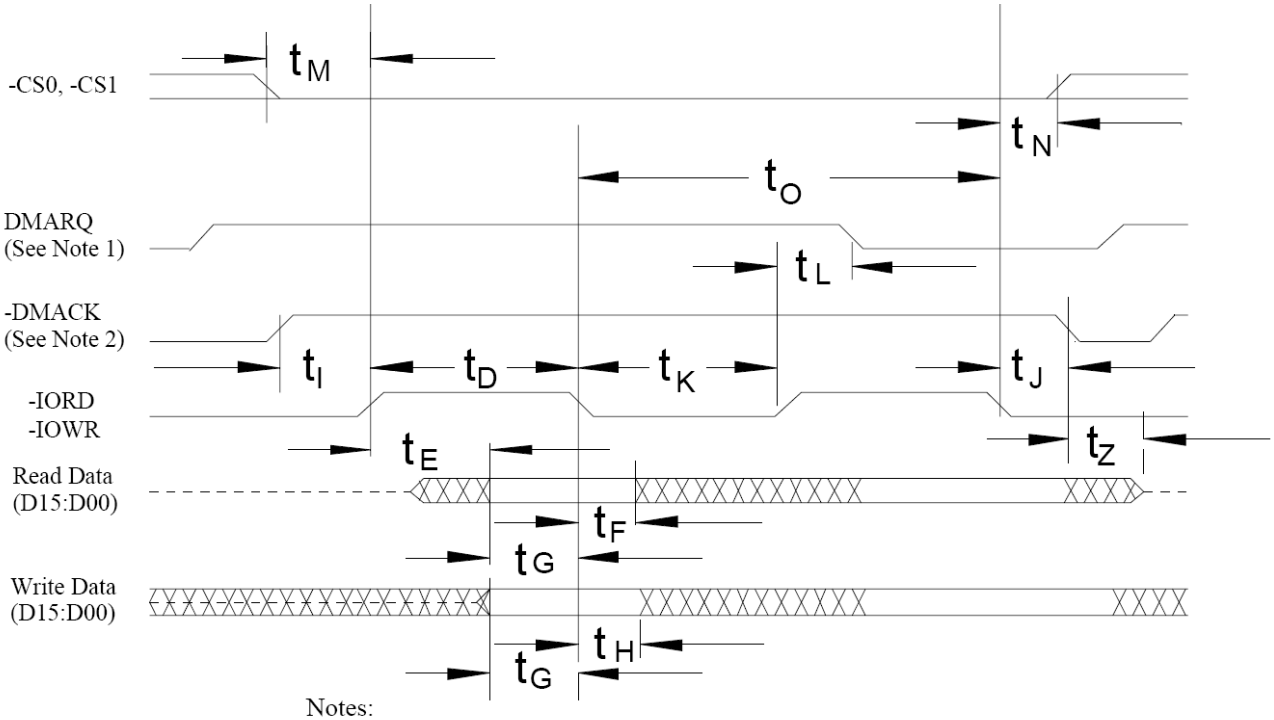
2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.

11.2 Multi Word DMA



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

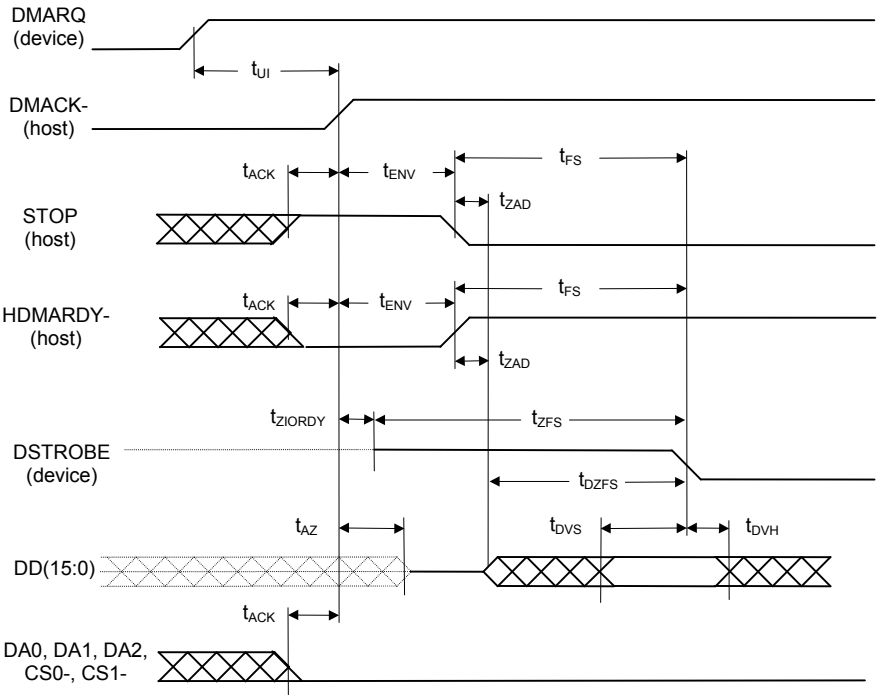
(2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

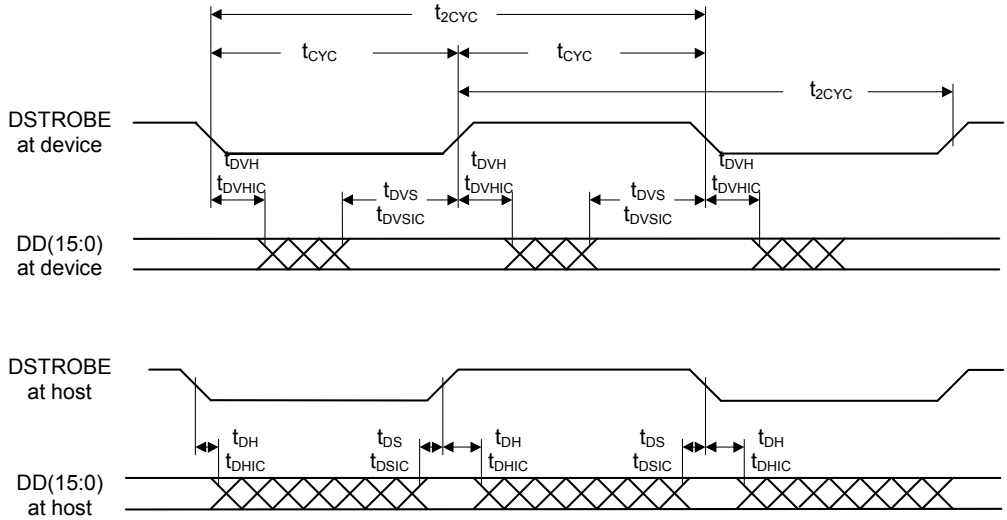
Multiword DMA timing parameters		Mode 0 (ns)	Mode 1 (ns)	Mode2 (ns)	Note
t_0	Cycle time (min)	480	150	120	See note
t_D	DIOR-/DIOW- asserted pulse width (min)	215	80	70	See note
t_E	DIOR- data access (max)	150	60	50	
t_F	DIOR- data hold (min)	5	5	5	
t_G	DIOR-/DIOW- data setup (min)	100	30	20	
t_H	DIOW- data hold (min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup (min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold (min)	20	5	5	
t_{KR}	DIOR- negated pulse width (min)	50	50	25	See note
t_{KW}	DIOW- negated pulse width (min)	215	50	25	See note
t_{LR}	DIOR- to DMACK delay (max)	120	40	35	
t_{LW}	DIOW- to DMACK delay (max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW- (min)	50	30	25	
t_N	CS(1:0) hold (min)	15	10	10	
t_Z	DMACK- to read data released (max)	20	25	25	
Notes- t_0 is the minimum total cycle. t_D is the minimum DIOR-/DIOW- assertion time, and t_K(t_{KR} or t_{KW}, as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.					

11.3 Ultra DMA

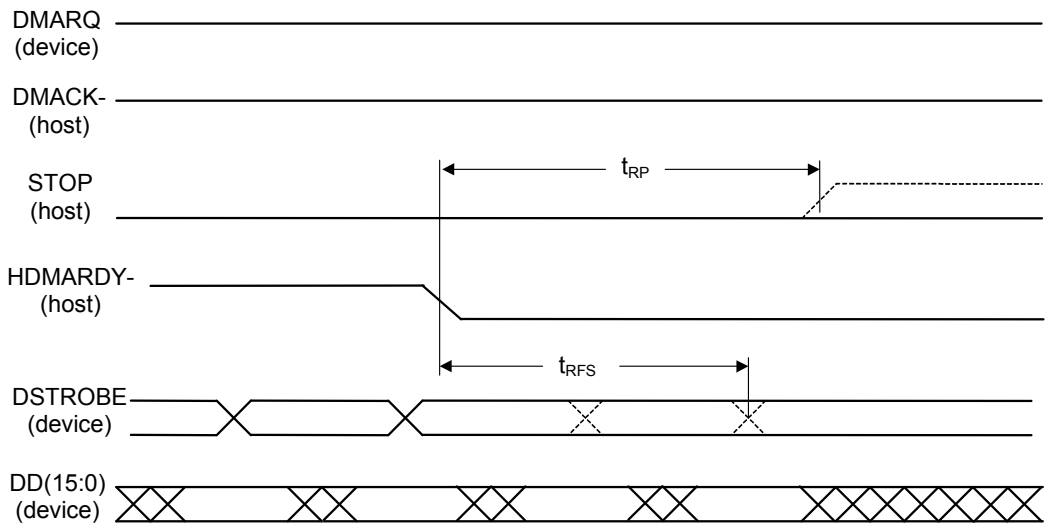
[Initiating an Ultra DMA data-in burst]



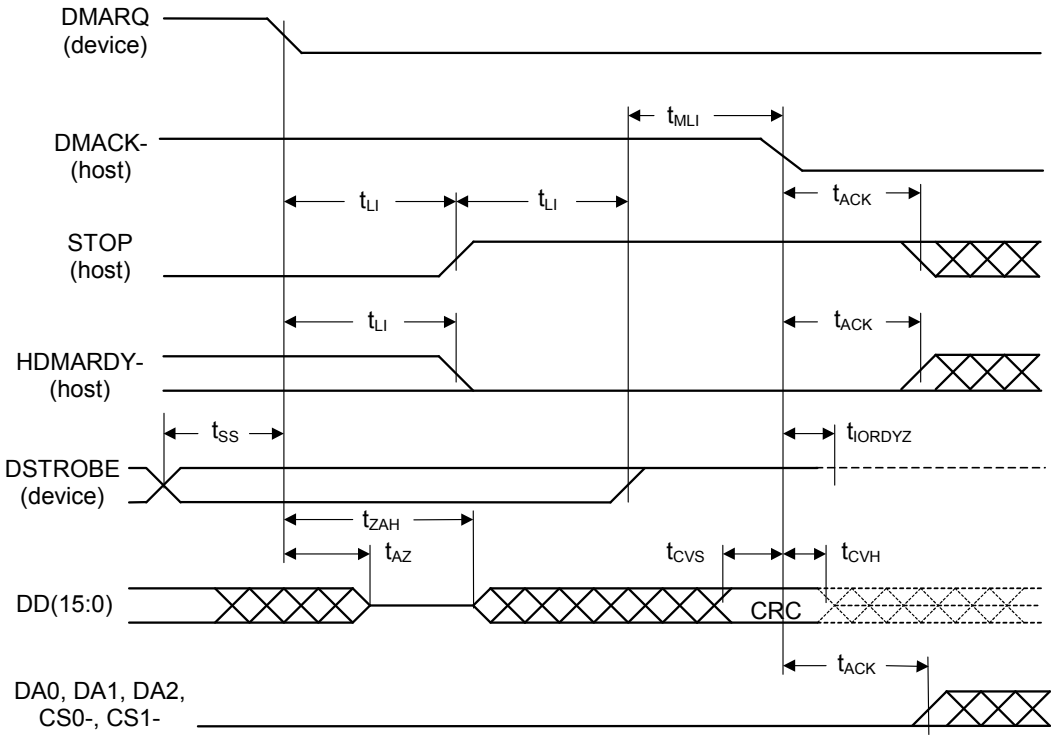
[Sustained Ultra DMA data-in burst]



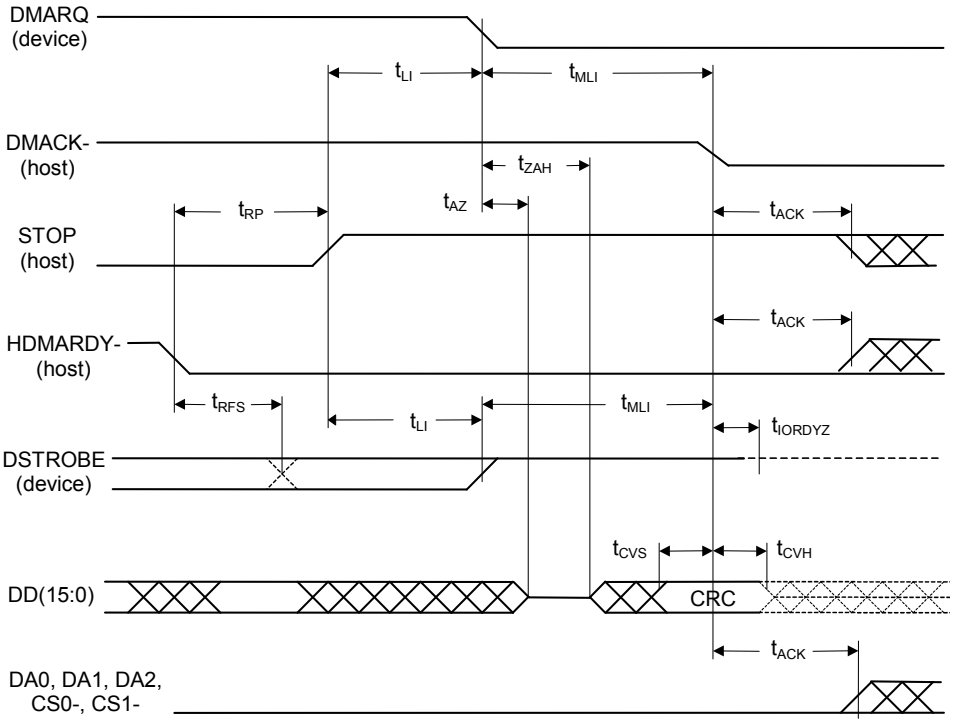
[Host pausing an Ultra DMA data-in burst]



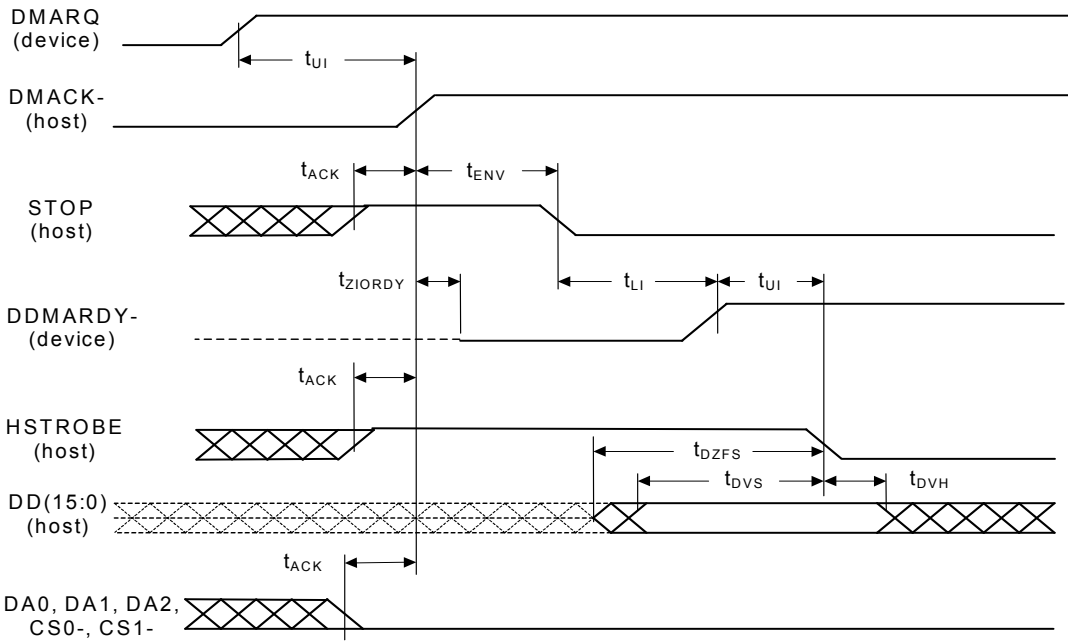
[Device terminating an Ultra DMA data-in burst]



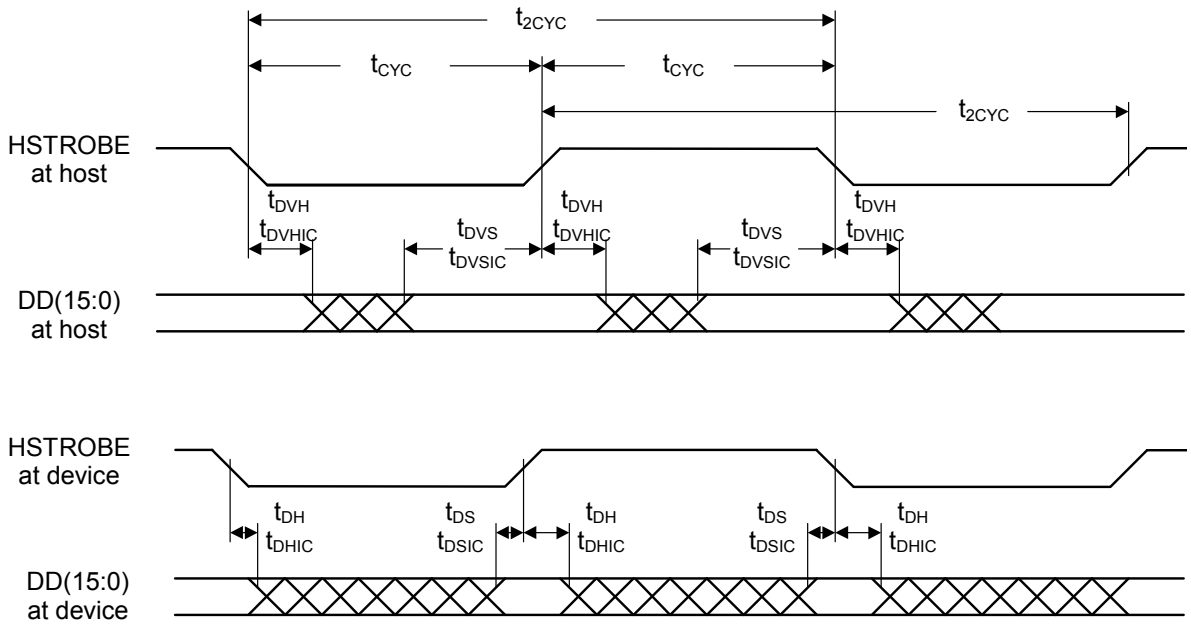
[Host terminating an Ultra DMA data-in burst]



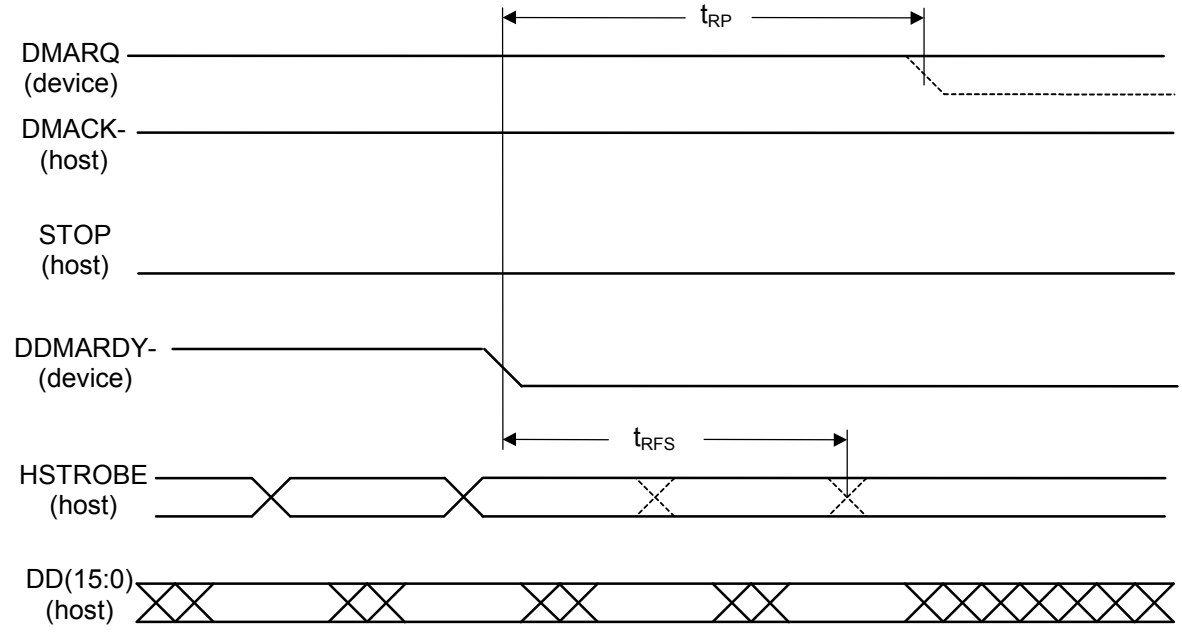
[Initiating an Ultra DMA data-out burst]



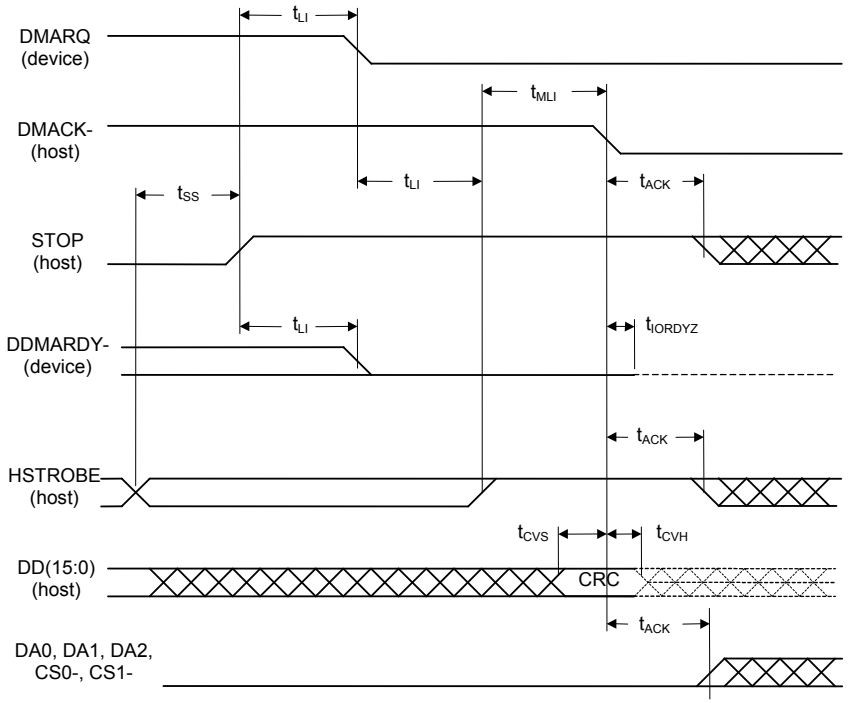
[Sustained Ultra DMA data-out burst]



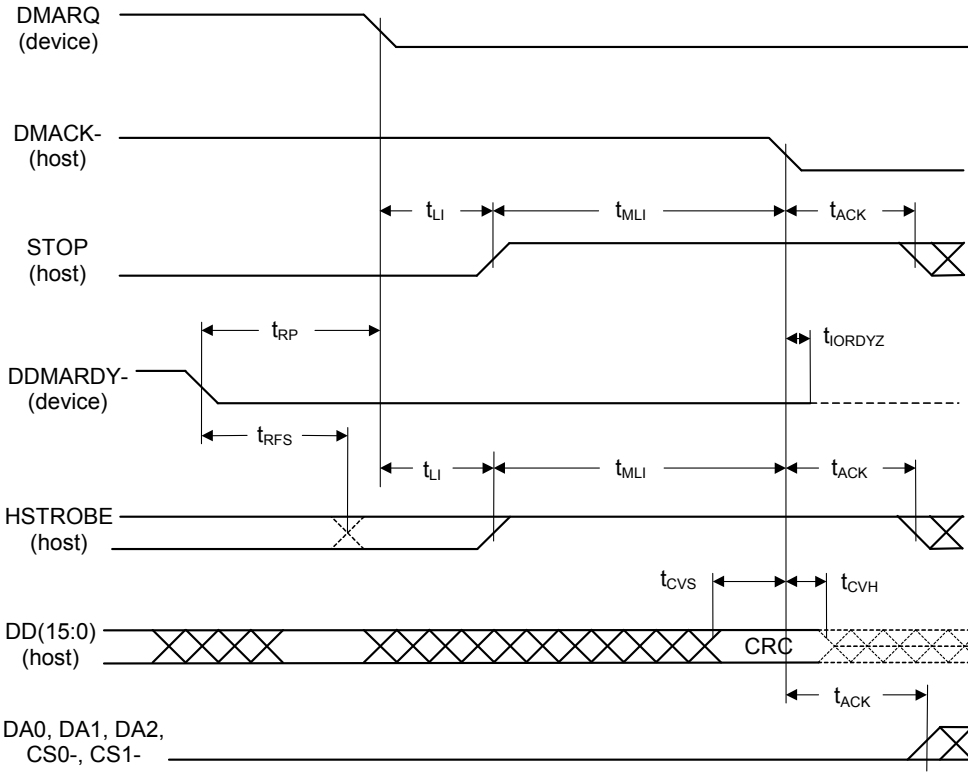
[Device pausing an Ultra DMA data-out burst]



[Host terminating an Ultra DMA data-out burst]



[Device terminating an Ultra DMA data-out burst]



[Ultra DMA data burst timing requirements]

Name	Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		Mode 3 (ns)		Mode 4 (ins)		Mode 5 (ns)		Measurement location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		Sender
t_{CYC}	112		73		54		39		25		16.8		Note 3
t_{2CYC}	230		153		115		86		57		38		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		Host
t_{ZFS}	0		0		0		0		0		35		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		Sender
t_{FS}		230		200		170		130		120		90	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Note 4
t_{MLI}	20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Host
t_{RFS}		75		70		60		60		60		50	Sender
t_{RP}	160		125		100		100		100		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		Sender

NOTES –

1 All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and DMARDY- transitions are measured at the sender connector.

3 The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4 The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5 The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

[Ultra DMA data burst timing descriptions]

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge) (See note 2,5)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid) (See note 2,5)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge) (See note 3)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid) (See note 3)
t_{CS}	CRC word setup time at device (See note 2)
t_{CH}	CRC word hold time device (See note 2)
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK- negation) (See note 3)
t_{CVH}	CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (See note 3)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time (See note 1)
t_{MLI}	Interlock time with minimum (See note 1)
t_{UI}	Unlimited interlock time (See note 1)
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY (See note 4)
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

NOTES –

1 The parameters t_{UI}, t_{MLI}, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2 80-conductor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

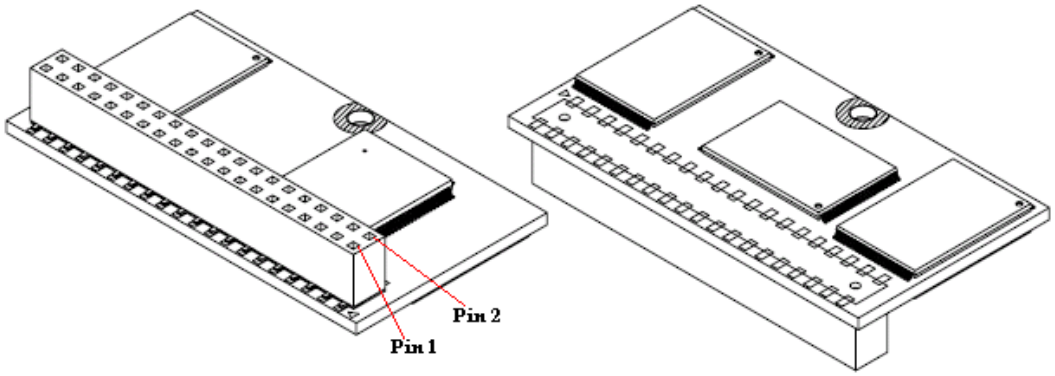
3 Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

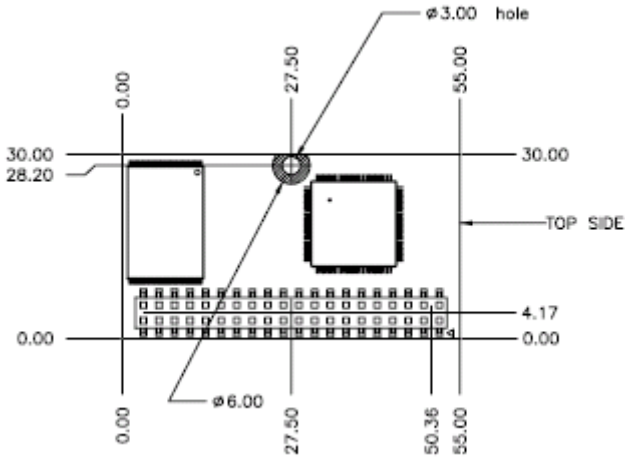
4 For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

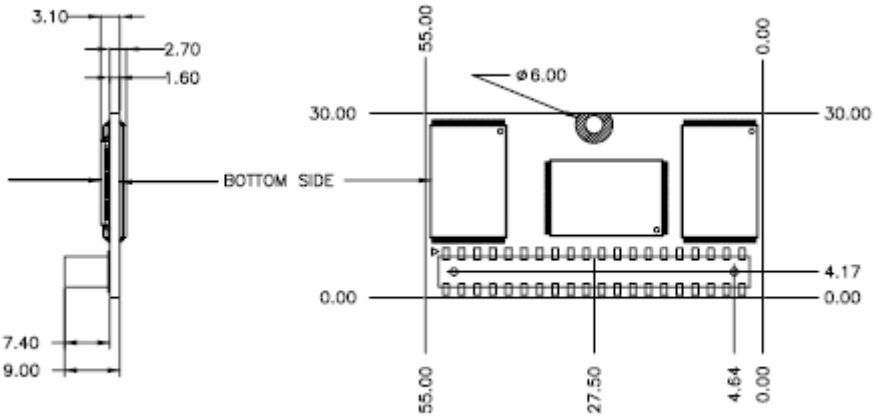
5 The parameters t_{DS}, t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

12. Physical Dimension

12.1 40-pin PDM Horizontal Top (Unit: mm)



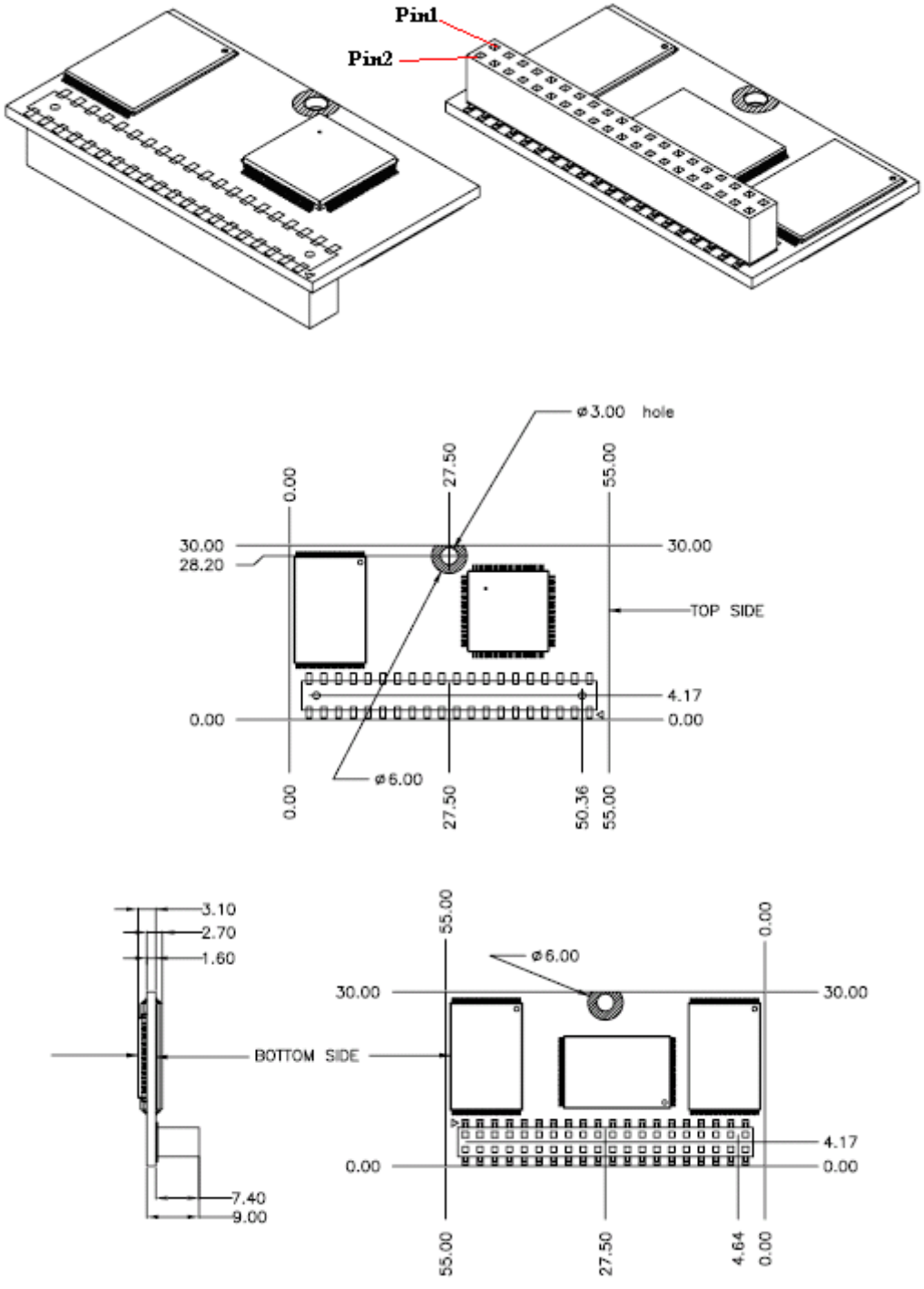




***Note：**

1. General Tolerance：± 0.1

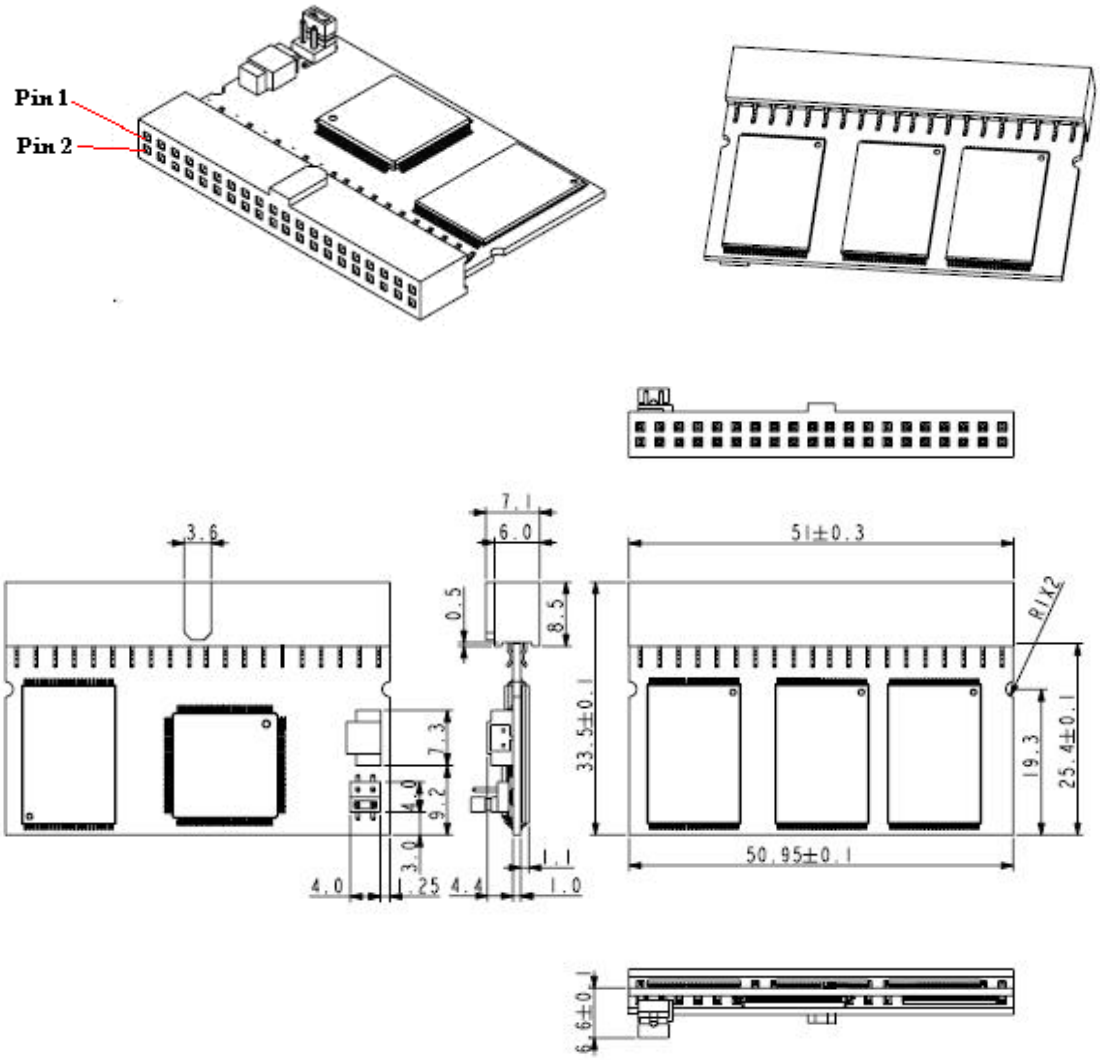
12.2 40-pin PDM Horizontal Bottom (Unit: mm)



***Note：**

1. General Tolerance：± 0.1

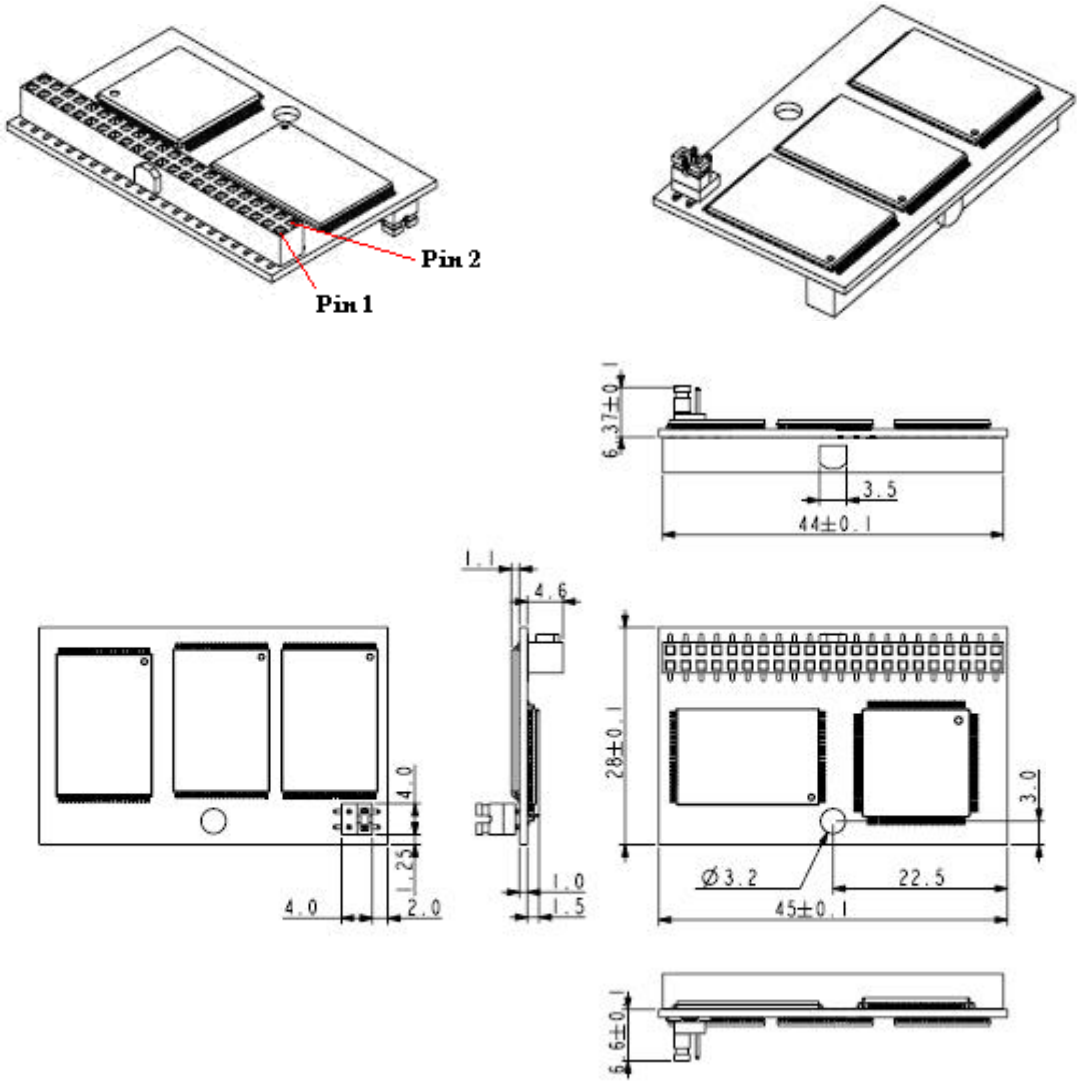
12.3 40-pin PDM Vertical (Unit: mm)



***Note：**

1. General Tolerance：± 0.1

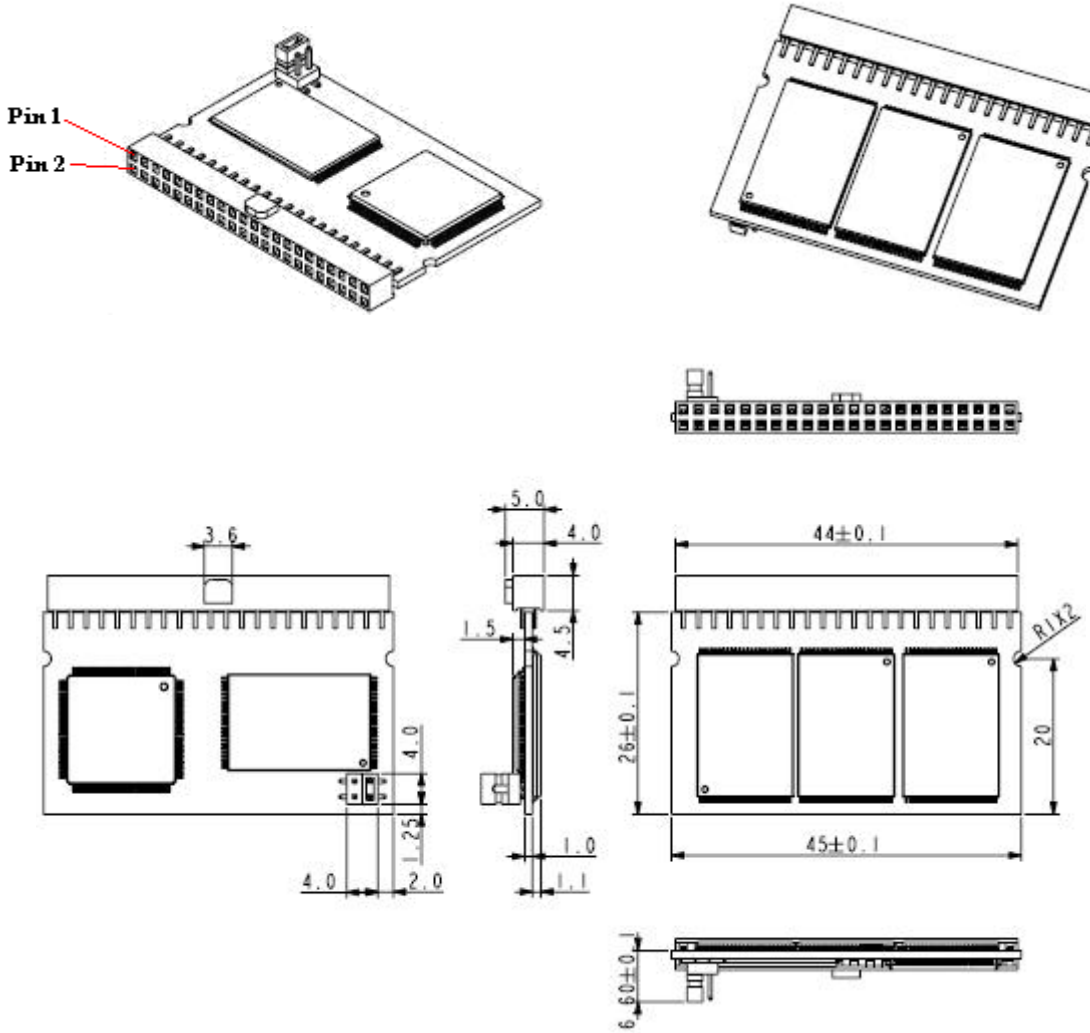
12.4 44-pin PDM Horizontal (Unit: mm)



***Note：**

1. General Tolerance：± 0.1

12.5 44-pin PDM Vertical (Unit: mm)



***Note：**

1. General Tolerance：± 0.1

Appendix: Part Number Table

A. 40-pin PDM Part Number：

Product	Advantech PN	Manufacture PN
Advantech SQFlash PDM 1G SLC 40-pin Horizontal Top (0~70°C)	SQF-PDMS1-1G-HBCE	PAB001GTSC0-P60
Advantech SQFlash PDM 2G SLC 40-pin Horizontal Top (0~70°C)	SQF-PDMS2-2G-HBCE	PAB002GTSC0-P60
Advantech SQFlash PDM 4G SLC 40-pin Horizontal Top (0~70°C)	SQF-PDMS2-4G-HBCE	PAB004GTSC0-P60
Advantech SQFlash PDM 8G SLC 40-pin Horizontal Top (0~70°C)	SQF-PDMS2-8G-HBCE	PAB008GTSC0-P60
Advantech SQFlash PDM 16G SLC 40-pin Horizontal Top (0~70°C)	SQF-PDMS2-16G-HBCE	PAB016GTSC0-P60
Advantech SQFlash PDM 1G SLC 40-pin Horizontal Top (-40~85°C)	SQF-PDMS1-1G-HBEE	PAB001GTSE0-P60
Advantech SQFlash PDM 2G SLC 40-pin Horizontal Top (-40~85°C)	SQF-PDMS2-2G-HBEE	PAB002GTSE0-P60
Advantech SQFlash PDM 4G SLC 40-pin Horizontal Top (-40~85°C)	SQF-PDMS2-4G-HBEE	PAB004GTSE0-P60
Advantech SQFlash PDM 8G SLC 40-pin Horizontal Top (-40~85°C)	SQF-PDMS2-8G-HBEE	PAB008GTSE0-P60
Advantech SQFlash PDM 16G SLC 40-pin Horizontal Top (-40~85°C)	SQF-PDMS2-16G-HBEE	PAB016GTSE0-P60
Advantech SQFlash PDM 1G SLC 40-pin Horizontal Bottom (0~70°C)	SQF-PDMS1-1G-HCCE	PAE001GTSC0-P60
Advantech SQFlash PDM 2G SLC 40-pin Horizontal Bottom (0~70°C)	SQF-PDMS2-2G-HCCE	PAE002GTSC0-P60
Advantech SQFlash PDM 4G SLC 40-pin Horizontal Bottom (0~70°C)	SQF-PDMS2-4G-HCCE	PAE004GTSC0-P60
Advantech SQFlash PDM 8G SLC 40-pin Horizontal Bottom (0~70°C)	SQF-PDMS2-8G-HCCE	PAE008GTSC0-P60
Advantech SQFlash PDM 16G SLC 40-pin Horizontal Bottom (0~70°C)	SQF-PDMS2-16G-HCCE	PAE016GTSC0-P60
Advantech SQFlash PDM 1G SLC 40-pin Horizontal Bottom (-40~85°C)	SQF-PDMS1-1G-HCEE	PAE001GTSE0-P60
Advantech SQFlash PDM 2G SLC 40-pin Horizontal Bottom (-40~85°C)	SQF-PDMS2-2G-HCEE	PAE002GTSE0-P60
Advantech SQFlash PDM 4G SLC 40-pin Horizontal Bottom (-40~85°C)	SQF-PDMS2-4G-HCEE	PAE004GTSE0-P60
Advantech SQFlash PDM 8G SLC 40-pin Horizontal Bottom (-40~85°C)	SQF-PDMS2-8G-HCEE	PAE008GTSE0-P60
Advantech SQFlash PDM 16G SLC 40-pin Horizontal Bottom (-40~85°C)	SQF-PDMS2-16G-HCEE	PAE016GTSE0-P60
Advantech SQFlash PDM 1G SLC 40-pin Vertical (0~70°C)	SQF-PDMS1-1G-VBCE	PAA001GTSC0-P60
Advantech SQFlash PDM 2G SLC 40-pin Vertical (0~70°C)	SQF-PDMS2-2G-VBCE	PAA002GTSC0-P60
Advantech SQFlash PDM 4G SLC 40-pin Vertical (0~70°C)	SQF-PDMS2-4G-VBCE	PAA004GTSC0-P60
Advantech SQFlash PDM 8G SLC 40-pin Vertical (0~70°C)	SQF-PDMS2-8G-VBCE	PAA008GTSC0-P60
Advantech SQFlash PDM 16G SLC 40-pin Vertical (0~70°C)	SQF-PDMS2-16G-VBCE	PAA016GTSC0-P60
Advantech SQFlash PDM 1G SLC 40-pin Vertical (-40~85°C)	SQF-PDMS1-1G-VBEE	PAA001GTSE0-P60
Advantech SQFlash PDM 2G SLC 40-pin Vertical (-40~85°C)	SQF-PDMS2-2G-VBEE	PAA002GTSE0-P60
Advantech SQFlash PDM 4G SLC 40-pin Vertical (-40~85°C)	SQF-PDMS2-4G-VBEE	PAA004GTSE0-P60
Advantech SQFlash PDM 8G SLC 40-pin Vertical (-40~85°C)	SQF-PDMS2-8G-VBEE	PAA008GTSE0-P60
Advantech SQFlash PDM 16G SLC 40-pin Vertical (-40~85°C)	SQF-PDMS2-16G-VBEE	PAA016GTSE0-P60

B. 44-pin PDM Part Number：

Product	Advantech PN	Manufacture PN
Advantech SQFlash PDM 1G SLC 44-pin Horizontal (0~70°C)	SQF-PDMS1-1G-HACE	PAD001GTSC0-P60
Advantech SQFlash PDM 2G SLC 44-pin Horizontal (0~70°C)	SQF-PDMS2-2G-HACE	PAD002GTSC0-P60
Advantech SQFlash PDM 4G SLC 44-pin Horizontal (0~70°C)	SQF-PDMS2-4G-HACE	PAD004GTSC0-P60
Advantech SQFlash PDM 8G SLC 44-pin Horizontal (0~70°C)	SQF-PDMS2-8G-HACE	PAD008GTSC0-P60
Advantech SQFlash PDM 16G SLC 44-pin Horizontal (0~70°C)	SQF-PDMS2-16G-HACE	PAD016GTSC0-P60
Advantech SQFlash PDM 1G SLC 44-pin Horizontal (-40~85°C)	SQF-PDMS1-1G-HAEE	PAD001GTSE0-P60
Advantech SQFlash PDM 2G SLC 44-pin Horizontal (-40~85°C)	SQF-PDMS2-2G-HAEE	PAD002GTSE0-P60
Advantech SQFlash PDM 4G SLC 44-pin Horizontal (-40~85°C)	SQF-PDMS2-4G-HAEE	PAD004GTSE0-P60
Advantech SQFlash PDM 8G SLC 44-pin Horizontal (-40~85°C)	SQF-PDMS2-8G-HAEE	PAD008GTSE0-P60
Advantech SQFlash PDM 16G SLC 44-pin Horizontal (-40~85°C)	SQF-PDMS2-16G-HAEE	PAD016GTSE0-P60
Advantech SQFlash PDM 1G SLC 44-pin Vertical (0~70°C)	SQF-PDMS1-1G-VACE	PAC001GTSC0-P60
Advantech SQFlash PDM 2G SLC 44-pin Vertical (0~70°C)	SQF-PDMS2-2G-VACE	PAC002GTSC0-P60
Advantech SQFlash PDM 4G SLC 44-pin Vertical (0~70°C)	SQF-PDMS2-4G-VACE	PAC004GTSC0-P60
Advantech SQFlash PDM 8G SLC 44-pin Vertical (0~70°C)	SQF-PDMS2-8G-VACE	PAC008GTSC0-P60
Advantech SQFlash PDM 16G SLC 44-pin Vertical (0~70°C)	SQF-PDMS2-16G-VACE	PAC016GTSC0-P60
Advantech SQFlash PDM 1G SLC 44-pin Vertical (-40~85°C)	SQF-PDMS1-1G-VAEE	PAC001GTSE0-P60
Advantech SQFlash PDM 2G SLC 44-pin Vertical (-40~85°C)	SQF-PDMS2-2G-VAEE	PAC002GTSE0-P60
Advantech SQFlash PDM 4G SLC 44-pin Vertical (-40~85°C)	SQF-PDMS2-4G-VAEE	PAC004GTSE0-P60
Advantech SQFlash PDM 8G SLC 44-pin Vertical (-40~85°C)	SQF-PDMS2-8G-VAEE	PAC008GTSE0-P60
Advantech SQFlash PDM 16G SLC 44-pin Vertical (-40~85°C)	SQF-PDMS2-16G-VAEE	PAC016GTSE0-P60